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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,210	01/29/2004	Yong-Kwan Lee	2557-000202/US	3354

7590 02/23/2006

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,210	LEE ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,16 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,16 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 01/06/2006 has been reviewed and placed of record in the file.

2. Applicant's arguments with respect to amended claims 1-4, 16, and 31-33, filed 01/06/2006, and with respect to the rejection over Yoshikawa JP 10-242355 in view of Caletka et al. U.S. Patent 6,507,116 have been considered but they are moot in view of new ground(s) of rejection. Applicant's arguments with respect to amended claims 1-4, 16, and 31-33, filed 01/06/2006, and with respect to the rejection over Caletka et al. U.S. Patent 6,507,116 in view of Yoshikawa JP 10-242355 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 1-4, 16, and 31-33** are rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshikawa JP 10-242355 (submitted by Applicant and cited by the Korean Industrial Property Office; Citations hereinafter using the translated version and simply referred to as the '355 reference) in view of Xu U.S. Patent Application Publication 20030143382 (the '382 reference).

The '355 reference discloses in the figures, particularly Fig. 2(b) and respective portions of the specification a flip-chip package substantially as claimed.

Referring to **claim 1**, the '355 reference discloses a flip chip package comprising:

a semiconductor chip (3) having a first side and a second side opposing the first side;

a circuit substrate (4) electrically connected to the first side of the semiconductor chip;

a protective cap (1) disposed over the second side of the semiconductor chip, the protective cap including at least one portion extending beyond an edge of the semiconductor chip, the portion including a groove having a fan-shaped cross-section such that a part of the groove further from the second side of the semiconductor chip is wider in cross-section than a part of the groove closer to the second side of the semiconductor chip; and

a molding resin layer (2) sealing the electrical connection between the semiconductor chip and the circuit substrate and filling the fan-shaped groove in the cap.

However, the '355 reference does not teach an adhesion layer disposed between an entirety of the second side of the semiconductor chip and at least a portion of the protective cap. As a matter of fact, the reference appears to be silent as to the material for the space between the second side of the semiconductor chip 3 and the protective cap 1 (see the figures, particularly Fig. 2b).

The '382 reference, in also disclosing a flip chip package a semiconductor chip (102, Fig. 1 or 402, Fig. 4) and a protective cap 104 or 404, and a space between the second (upper) side of the semiconductor chip and the protective cap, teaches that the space between the second side of the semiconductor chip and the protective cap ("the lower surface of the thermally conductive member") be filled with thermally conductive material, also known as TIM – thermal interface material - in the art, or an adhesive for short, utilizing covalent bonding to reduce thermal resistance across an interface between the semiconductor chip and the protective cap (paragraph

[0011]. Thus, the '382 reference appears to literally truly teach that the adhesion layer be disposed on the entirety, down to the molecular level, of the second side of the semiconductor chip.

Therefore, it would have been obvious to form the '355 reference's device such that an adhesion layer is disposed between an entirety of the second side of the semiconductor chip and at least a portion of the protective cap. One would have been motivated to make such a change in view of the teachings in Xu that such a change promotes reduced thermal resistance across an interface between the semiconductor chip and the protective cap.

Referring to **claims 2-3**, although the '355 reference does not disclose that the protective cap/heat spreader includes a metal such as copper or aluminum, the selection of copper and aluminum as heat spreader (i.e., heat sink, heat releasing,...) at the time the invention was made still within routine skill of a person of ordinary skill in the art, therefore such selection would have been obvious.

Referring to **claim 4**, the '355 reference further discloses a plurality of solders (6) to electrically connect the semiconductor chip and the circuit substrate.

Referring to **claim 16**, the '355 reference further discloses solder balls (5) formed on a surface of the circuit substrate opposite a surface to which the circuit substrate is electrically connected to the semiconductor chip.

Referring to **claim 31**, the '355 reference further discloses that the protective cap includes more than one portion extending beyond an edge of the semiconductor chip, and each portion includes a groove having a fan-shaped cross-section; and that the molding resin layer fills each groove.

Referring to **claim 32**, the '355 reference further discloses that the groove is formed through the protective cap (Fig. 2b).

Referring to **claim 33**, the '355 reference further discloses that the groove is not formed through the cap (Fig. 5).

4. **Claims 1-4, 16, and 31-33** are rejected under 35 U.S.C. §103(a) as being unpatentable over Caletka et al. U.S. Patent 6,507,116 (the '116 reference, cited in a previous office action) in view of Yoshikawa JP 10-242355 (submitted by Applicant and cited by the Korean Industrial Property Office; Citations hereinafter using the translated version and simply referred to as the '355 reference).

The '116 reference discloses in Fig. 4 and other figures, with the other figures showing the elementary components in more details, and respective portion of the specification a flip chip package substantially as claimed.

Referring to **claim 1**, the '116 reference discloses a flip chip package comprising:

a semiconductor chip (no number, whose side surface is indicated as 220) having a first side and a second side opposing the first side;

a circuit substrate ("circuitized substrate", indicated as 16 in Fig. 1 and as 216 in Fig. 4) electrically connected to the first side of the semiconductor chip;

a protective cap ("thermally conductive member" 222, Fig. 4, column 6, lines 31-47, and note that although the reference does not explicitly disclose that element 222 is a protective cap, it is a protective cap as it protects the chip from the environmental elements) disposed over the second side of the semiconductor chip, the protective cap including at least one portion extending beyond an edge of the semiconductor chip (as is evident from the figures), the portion including a groove ("opening" 229);

a molding resin layer (226) sealing the electrical connection between the semiconductor chip and the circuit substrate and filling the groove in the cap; and

an adhesion layer disposed between an entirety of the second side of the semiconductor chip and at least a portion of the protective cap (Fig. 4, column 8, lines 49-55: "The lower surface of the thermally conductive member can be placed on the planar upper surface of the chip with thermally conductive material, or an adhesive.").

However, the reference does not teach that the groove has a fan-shaped cross-section such that a part of the groove further from the second side of the semiconductor chip is wider in cross-section than a part of the groove closer to the second side of the semiconductor chip.

Yoshikawa in the '355 reference, in also disclosing a flip chip package including groove (1B, 1D, Figs. 2's and 5) having a fan-shaped cross-section such that a part of the groove further from the second side of the semiconductor chip is wider in cross-section than a part of the groove closer to the second side of the semiconductor chip and/or a hook structure 1A, teaches that such a modification reduces exfoliation and crack in the flip chip package, specifically at the interface and the boundary (page 4 and paragraph [0036], page 14).

Therefore, it would have been obvious to form the '116 reference's device such that the groove 229 has a fan-shaped cross-section such that a part of the groove further from the second side of the semiconductor chip is wider in cross-section than a part of the groove closer to the second side of the semiconductor chip. One would have been motivated to make such a change in view of the teachings in Yoshikawa that such a change reduces exfoliation and crack in the flip chip package, specifically at the interface and the boundary.

Referring to **claims 2-3**, the '116 reference further discloses that the thermally conductive protective cap 222, similar to the thermally conductive protective cap 22, includes metal and is

made of one selected from the group consisting of copper (Cu), copper alloy, aluminum (Al), and aluminum alloy (column 5, lines 5-10).

Referring to **claim 4**, the '116 reference further discloses a plurality of solders (214) to electrically connect the semiconductor chip and the circuit substrate.

Referring to **claim 16**, the '116 reference further discloses solder balls (not shown in the circuit substrate 216 of Fig. 4, shown as balls at a lower surface of the circuit substrate 16 of Fig. 1) formed on a surface of the circuit substrate opposite a surface to which the circuit substrate is electrically connected to the semiconductor chip.

Referring to **claim 31**, the '355 reference further discloses that the protective cap includes more than one portion extending beyond an edge of the semiconductor chip, and each portion includes a groove having a fan-shaped cross-section; and that the molding resin layer fills each groove.

Referring to **claim 32**, both the references further disclose that the groove is formed through the protective cap (groove 229 in Fig. 4, the '116 reference; groove 1B in Fig. 2b, the '355 reference).

Referring to **claim 33**, the '335 reference further discloses that the groove (1D) is not formed through the cap (Fig. 5).

Response to Arguments

5. In response to applicant's argument on Page 5 of 8, Remark filed 01/06/2006, that the adhesion layer of a non-preferred embodiment of the '116 reference (Caletka) is not applied across the entirety of the semiconductor chip, it is respectfully pointed out that the adhesion layer

(no number, Fig. 4, column 8, lines 49-55: "The lower surface of the thermally conductive member can be placed on the planar upper surface of the chip with thermally conductive material, or an adhesive.") of the '116 reference (Caletka) is applied across the entirety of the semiconductor chip. While it is true that the '116 reference states in col. 5, lines 52-55, that "a small space may be left between the lower surface of the thermally conductive member and the planar upper surface of the chip without thermally conductive material present", it is believed that this statement is directed to the preferred embodiments (Fig. 5A, for example, and col. 8, last paragraph), and not to the non-preferred embodiment, that of Fig. 4, which is relied on by the examiner.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
February 17, 2006